DR. SANDEEP MISHRA

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Professional Experience

Position	Employer	Last Basic Pay	Duration
Assistant Professor (Grade-I)	SVNIT Surat	101500 (Basic)	Oct 2023–Present
Assistant Professor (Grade-II)	IIIT Pune	75300 (Basic)	Jan 2020–Oct 2023
Assistant Professor	IIIT Pune	70000 (Cons.)	Jul 2018–Jan 2020
Assistant Professor	NIT Sikkim	65000 (Cons.)	Feb 2018–Jul 2018
Lecturer	GIET University	19400 (Cons.)	Jul 2013–Jul 2014
		Total Teaching Experience = 6 years	

Awards and Achievements

- *2016*: Best paper award at *TechSym-2016 conference* for late breaking research presentation
- *2011*: Best designer for student project (Function Generator)
- *2004*: NRTS matching scholarship
- *2002*: Orissa state talent scholarship examination

Sponsored Project

Title	Type	Agency	Amount	Duration	Role	Status
Secure and Energy Efficient Mixed Domain Compute in Memory-based AI Accelerator Chip for Edge Applications	Externally Sponsored	MeitY, Govt. of India	INR 96.5 Lakhs	5 years	Co-Chief Investigator	Ongoing (Start: 2024)
Power and Space optimization in Internet of Things (IoT) System-on-Chip (SoC)	Externally Sponsored	MeitY, Govt. of India	INR 81.5 Lakhs	5 years	Investigator	Ongoing (Start: 2023)

Publication Summary

Journals	Conferences	Book Chapters	h-index	i-10 index
17 (SCI/SCIE)	12	2	9	8

Key Administrative Responsibilities

- Faculty In-Charge, Center for Continuing Education, SVNIT Surat
- Head of Department, Electronics and Communication Engineering, IIIT Pune
- Assistant Registrar (I/C), IIIT Pune
- Chairman, Purchase Committee, IIIT Pune
- Member, Internal Complaints Committee, IIIT Pune

Courses Taught

- Introduction to VLSI Design
- Digital Logic Design
- Microprocessors & Microcontrollers
- Computer Architecture & Organization
- Embedded System
- Digital System Design

Invited Lectures

Topic	Workshop/Course/Training	Organization	Duration
Digital System Design	Student Training Program	CSVTU, Bhilai	13-16 Mar. 2021
VLSI Design	Student Training Program	CSVTU, Bhilai	23-27 Sep. 2020
Evolution of Memories – from RAM to CAM	Nanoscale Devices: Materials to Applications	Electronics & ICT Academy, MNIT Jaipur	08 Nov. 2019

Workshops/ Seminars/ Courses/ Conferences Organized:

Title	Event Category	Organization	Role	Duration
Custom IC Design using EDA	Abhyaas – Karyashala	Science & engineering research board (SERB)	Coordinator	27 Feb – 5 Mar 2022
Custom IC Design in the Advanced CMOS Technology	Faculty development program	ATAL academy (AICTE)	Coordinator	21 Nov – 25 Nov. 2021

Key Publications

- S. W. Hussain, T. V. Mahendra, **S. Mishra**, and A. Dandapat, "Content-Addressable Memory using Selective-Charging and Adaptive-Discharging Scheme for Low-Power Hardware Search Engine," *Integration, the VLSI Journal*, pp. 1-13, May 2024. (*Accepted*)
- S. W. Hussain, T. V. Mahendra, **S. Mishra**, and A. Dandapat, "SMS-CAM: Shared Matchline Scheme for Content Addressable Memory," *Integration, the VLSI Journal*, vol. 88, pp. 70-79, Jan. 2023.
- S. W. Hussain, T. V. Mahendra, **S. Mishra**, and A. Dandapat, "Match-line control unit for power and delay reduction in hybrid CAM," *IET Circuits, Devices & Systems*, vol. 15, no. 3, pp. 272-283, Feb. 2021.
- **S. Mishra**, T. V. Mahendra, S. W. Hussain, and A. Dandapat, "The analogy of matchline sensing techniques for content addressable memory (CAM)," *IET Computers & Digital Techniques*, vol. 14, no. 3, pp. 87-96, Apr. 2020.
- T. V. Mahendra, S. W. Hussain, **S. Mishra**, and A. Dandapat, "Energy-efficient precharge-free ternary content addressable memory (TCAM) for high search rate applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 67, no. 7, pp. 2345-2357, Jul. 2020.
- F. Begum, **S. Mishra**, N. Islam, and A. Dandapat, "A 10-bit 2.33 fJ/conv. SAR-ADC with high speed capacitive DAC switching using a novel effective asynchronous control circuitry," *Analog Integrated Circuits and Signal Processing*, vol. 100, no. 2, pp. 311-325, Aug. 2019.
- **S. Mishra**, T. V. Mahendra, J. Saikia, and A. Dandapat, "A low-overhead dynamic TCAM with pipelined read-restore refresh scheme," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 65, no. 5, pp. 1591-1601, May 2018.
- S. W. Hussain, T. V. Mahendra, **S. Mishra**, and A. Dandapat, "Match-line division and control to reduce power dissipation in content addressable memory," *IEEE Transactions on Consumer Electronics*, vol. 64, no. 3, pp. 301-309, Aug. 2018.
- **S. Mishra** and A. Dandapat, "Energy-efficient adaptive match-line controller for large-scale associative storage," *IEEE Transactions on Circuits and Systems II: Express Briefs*, vol. 64, no. 6, pp. 710-714, Jun. 2017.
- **S. Mishra**, T. V. Mahendra, and A. Dandapat, "A 9-T 833-MHz 1.72-fJ/bit/search quasi static ternary fully associative cache tag with selective matchline evaluation for wire speed applications," *IEEE Transactions on Circuits and Systems I: Regular Papers*, vol. 63, no. 11, pp. 1910-1920, Nov. 2016.
- **S. Mishra** and A. Dandapat, "EMDBAM: A low power dual bit associative memory with match error and mask control," *IEEE Transactions on Very Large Scale Integration (VLSI) Systems*, vol. 24, no. 6, pp. 2142-2151, Jun. 2016.